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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,158	03/19/2004	Yoshi Ono	SLA0830	8642

27518 7590 11/29/2005

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EXAMINER	
PIZARRO CRESPO, MARCOS D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/805,158	ONO ET AL.	
	Examiner	Art Unit	
	Marcos D. Pizarro-Crespo	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16,17 and 20-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16,17 and 20-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Attorney's Docket Number: SLA0830
Filing Date: 3/19/2004
Claimed Foreign Priority Date: none
Applicant(s): Ono, et al.
Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the amendment filed on 10/7/2005.

Acknowledgment

1. The amendment filed on 10/7/2005, responding to the Office action mailed on 7/26/2005, has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 16, 17, and 20-28.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 16, 17, 21, 22, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halliyal (US 6451641) in view of Tiwari (US 2004/0108537).

5. Regarding claim 16, Halliyal shows most aspects of the instant invention including a method of fabricating a non-volatile memory transistor comprising the steps of:

- ✓ Preparing a semiconductor substrate (see, *e.g.*, fig. 5/step S501)
- ✓ Forming a gate stack on the substrate as follows:
  - Depositing a high-k dielectric (see, *e.g.*, fig. 5/steo S502)
  - Forming an electrode layer overlying the dielectric (see, *e.g.*, fig. 5/step S503)
- ✓ Forming source/drain regions **104/106** on opposite sides of the gate stack (see, *e.g.*, fig. 1)

Halliyal, however, fails to show the step of forming the gate stack also comprising exposing the dielectric material to an ionized species that induce trapping centers in the dielectric. Tiwari, on the other hand, suggests exposing Halliyal's dielectric to an ionized species to incorporate trapping centers into the material (see, *e.g.*, par. 0065). Advantages include thinner gate dielectrics, long retention times, reasonably low power and high endurance (see, *e.g.*, par. 0004).

It would have been obvious at the time of the invention to one of ordinary skill in the art to expose Halliyal's dielectric material to an ionized species inducing trapping centers in the material, as suggested by Tiwari, so that long retention times can be obtained.

6. Regarding claim 17, Halliyal shows the high-K dielectric material comprising hafnium oxide (see, *e.g.*, col.6/ll.37).

7. Regarding claim 21, Halliyal/Tiwari show most aspects of the instant invention (see, *e.g.*, paragraph 5 above). Tiwari also teaches the step of exposing the dielectric includes exposing the dielectric to plasma to incorporate trapping sites into the layer (see, *e.g.*, par. 0065). Halliyal/Tiwari, however, fail to specify an exposure time of about 10-100 seconds. Although Halliyal/Tiwari fail to specify the time of duration of the plasma exposure, performing Tiwari's step would necessarily require a certain amount of time. The specification, on the other hand, fails to provide teachings about the criticality of having a specific plasma exposure time of 10-100 seconds. It has been held that time differences will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such time is critical. "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the workable ranges by routine experimentation". *In re Aller*, 220 F.2d 454,456,105 USPQ 233, 235 (CCPA 1955).

Since the applicants have not established the criticality (see next paragraph) of the exposure time claimed, it would have been obvious to one of ordinary skill in the art to use these values in the method of Halliyal/Tiwari.

CRITICALITY

8. The specification contains no disclosure of either the critical nature of the claimed exposure time or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

9. Regarding claim 22, Halliyal shows the trapping layer is deposited by an ALD method (see, *e.g.*, col.6/ll.33).

10. Regarding claim 25, Halliyal shows the substrate is an SOI substrate (see, *e.g.*, col.5/ll.66).

11. Regarding claim 26, Halliyal shows the transistor is a multi-bit transistor (see, *e.g.*, col.5/ll.20).

12. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Halliyal/Tiwari in view of Afanas'ev.

13. Regarding claim 20, Halliyal/Tiwari show most aspects of the instant invention (see, *e.g.*, paragraph 5 above), except for the step of exposing the dielectric including exposing the dielectric to nitrogen or hydrogen. Tiwari, however, teaches that the plasma exposure includes species that form trapping centers (see, *e.g.*, par. 0065). Afanas'ev teaches that nitrogen would increase the trapping sites in Halliyal/Tiwari's trapping layer and, therefore, would diminish the degrading impact of hole trapping (see, *e.g.*, pp.2525/col.2/ll.47-52).

It would have been obvious at the time of the invention to one of ordinary skill in the art to use nitrogen in the exposure step of Halliyal/Tiwari, as suggested by Afanas'ev, to diminish the degrading impact of hole trapping.

14. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Halliyal/Tiwari in view of Chooi (US 6486080) and Agarwal (US 2001/0015453).

15. Regarding claim 23, Halliyal/Tiwari shows most aspects of the instant invention (see, *e.g.*, paragraph 5 above), except for a densification anneal step after deposition of the charge-trapping layer. Chooi (see, *e.g.*, col.6/ll.5-7) and Agarwal (see, *e.g.*, par.0005/ll.5-10), on the other hand, suggest following the deposition of Halliyal's trapping layer with an anneal step to densify the layer by filling oxygen vacancies that develop in the layer during its formation.

It would have been obvious at the time of the invention to one of ordinary skill in the art to follow the deposition of Halliyal/Tiwari's trapping layer with the anneal step suggested by Chooi and Agarwal to cure oxygen vacancies developed in the layer during the deposition step.

16. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Halliyal/Tiwari in view of Liang (US 5372957).

17. Regarding claim 24, Halliyal/Tiwari shows most aspects of the instant invention (see, *e.g.*, paragraph 5 above) except for the formation of the drain and source regions comprising an angle source/drain implantation. Liang (see, *e.g.*, col.5/ll.4-7), on the other hand, teaches that angle implantation would place the ions further into the gate region of Halliyal/Tiwari's transistor without driving in the dopants. The resultant structure would be more immune to hot carrier degradation.

It would have been obvious at the time of the invention to one of ordinary skill in the art to form Halliyal/Tiwari's source/drain regions using the angle implantation suggested by Liang to protect the transistor against hot carrier degradation.

18. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Halliyal/Tiwari in view of Forbes (US 6140181).

Regarding claim 27, Halliyal/Tiwari shows most aspects of the instant invention (see, *e.g.*, paragraph 5 above). They however, fail to specify the ion energy and dose concentration of the ionized species.

Forbes, on the other hand, teaches that the energy is adjusted according to the distance from the substrate at which the species are to be localized (see, *e.g.*, col.4/ll.35-41). He also teaches that the dose concentration is adjusted to avoid agglomeration of point defect trap sites. In one embodiment the dose concentration is about 10^{15} atoms/cm^2 (see, e.g., col.4/ll.44-54).

Although the prior art does not show the claimed energy and implantation dose, *i.e.*, about 10-300 keV and about 10^{14}-10^{17}, respectively, absent any criticality, these are only considered to be the "optimum" values (see, *e.g.*, Forbes/col.4/ll.35-54) disclosed by Halliyal/Tiwari that a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired implantation distance, defect agglomeration, manufacturing costs, etc. (see Boesch, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results, *i.e.*, results which are different in kind and not in degree from the results of the prior art,

will be obtained as long as the dielectric is exposed to an ionized species, as already suggested by Halliyal/Tiwari.

In addition, it has been held that differences in distance and concentration will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such thickness and/or concentration are critical. "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the workable ranges by routine experimentation". *In re Aller*, 220 F.2d 454,456,105 USPQ 233, 235 (CCPA 1955).

Since the applicant has not established the criticality (see paragraph 8 above) of the claimed energy and dose, and since similar values have been previously used in the art (see, *e.g.*, Forbes/col.4/ll.50) it would have been obvious to one of ordinary skill in the art to use these values in the device of Halliyal/Tiwari.

19. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Halliyal/Tiwari in view of Moslehi (US 5372957).

20. Regarding claim 28, Halliyal/Tiwari shows most aspects of the instant invention (see, *e.g.*, paragraph 5 above). Tiwari also teaches the step of exposing the dielectric includes generating plasma (see, *e.g.*, par.0065). Halliyal/Tiwari, however, fail to show that generating the plasma includes using an inductively coupled plasma (ICP) source. Moslehi, on the other hand, suggests using an ICP source over other conventional plasma source due to its superior process performance, throughput rate, and control capabilities including its ability to control the plasma density and ion energy independent of each other (see, *e.g.*, col.1/ll.30-64).

It would have been obvious at the time of the invention to one of ordinary skill in the art to use an ICP source to generate the plasma of Halliyal/Tiwari, as suggested by Moslehi, because of its superior performance, throughput rate, and control capabilities.

Response to Arguments

21. The applicants argue:

> Halliyal mentions that his device may be used as a FET in an EEPROM memory. However, Halliyal does not describe either an NROM or MONOS memory device, or any kind of transistor that operates on a charge-trapping or floating gate principle. Moreover, Halliyal does not describe a device where charge can be trapped in a gate stack.

The examiner responds:

The claims of the instant invention broadly recite a method of fabricating a non-volatile memory transistor. The above features of the claimed invention, *i.e.*, NROM and MONOS memory devices, are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

22. The applicants argue:

> Tiwari only describes ion implantation as performed on a silicon nitride material. Silicon nitride material is a low-k dielectric material according to Halliyal (see, *e.g.*, col.3/ll.13-19). Tiwari never mentions that his process can be applicable to high-K dielectric materials. In addition, Halliyal does not describe a trapping layer for a memory transistor. Therefore, there is no support for the contention that Halliyal's dielectric can be modified to perform a completely different function (memory), based upon a process that is not even discussed in Tiwari (implantation of a high-k dielectric).

The examiner responds:

Halliyal clearly describes a memory transistor having a charge-trapping layer (see, *e.g.*, col.5/ll.14-22, col.6/ll.37); and Tiwari clearly teaches that his process is applicable to the same high-K dielectric materials taught by Halliyal (see, *e.g.*, Tiwari, par.0010).

23. The applicants argue:

> In his conclusions, Afanas'ev states that nitrogen impurities can be used to enhance electron trapping in Al_2O_3, ZrO_2, and HfO_2 materials. However, Afanas'ev never describes any type of implantation process. He only describes as-deposited nitrogen-containing films (see, *e.g.*, abstract). Therefore, it is not evident how Afanas'ev study of as-deposited impurities in high-k dielectrics suggests any modifications to Tiwari's implantation step. Likewise, there appears to be no suggestion to combine Afanas'ev as deposited impurities with Halliyal's process of protecting the high-k dielectric from reduction when the gate is formed.

The examiner responds:

One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In the instant case, Halliyal/Tiwari teaches exposing the dielectric to ionized impurities to form trapping centers (see, *e.g.*, Tiwari/par.0065). They, however, fail to specify the species. Afanas'ev teaches that nitrogen would increase the trapping sites in Halliyal/Tiwari's trapping layer and, therefore, would diminish the degrading impact of hole trapping (see, *e.g.*, pp.2525/col.2/ll.47-52). There is no teaching in Afanas'ev against the incorporation of nitrogen using the ion implantation of Tiwari. Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art to use nitrogen in the exposure step of Halliyal/Tiwari, as suggested by Afanas'ev, to diminish the degrading impact of hole trapping.

Conclusion

24. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

25. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

26. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(571) 273-8300**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(571) 272-1716** and between the hours of 9:30 AM to 8:00 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (571) 272-1705.

28. Any inquiry of a general nature or relating to the status of this application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status

information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

29. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/288,295,310,314,324-326,410,411	11/14/2005
Other Documentation:	
Electronic Database(s): EAST (USPAT, EPO, JPO)	11/14/2005

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